IN THE SPECIFICATION

Please amend the third full paragraph on page 11 as shown below:

-- The logic gate 60 is of a NOR type and has a first input terminal connected to the intermediate node 58, a second input terminal connected to the sixth input 22g and receiving the deactivation signal RESET, and an output terminal connected to the output 22a of the timing block 22 and supplying the pulse signal PS(i). In particular, the deactivation signal RESET is generated by an OR logic gate (not illustrated), which receives on a first input a signal PWDOWN for controlling switching-off of the read circuits of the memory device, said signal having the function of preventing spurious readings of the memory device, and on a second input the negated read signal $\overline{READ}$.--

Please insert the equation shown below on page 13, line 19:

$$--T_{ON}(i) = \frac{C_{LOAD}(i) * (V_{GATE} - V_{TH}) * K}{I_{MIR}}--$$

Please amend the second full paragraph on page 13 as shown below:

--In this step, the negated read signal $\overline{READ}$ goes to a low logic level, and, since the signal PWDOWN is also at a low logic level, the RESET signal supplied by the OR logic gate (not illustrated) goes to a low logic level--